REMARKS

Claims 1 - 8, 12, 14 - 34 are pending in the present application, of which claims 15 - 34 have been withdrawn from consideration. By this Amendment, claims 2 and 36 have been amended. No new matter has been added. It is believed that this amendment is fully responsive to the Office Action dated October 2, 2002.

Allowable Subject Matter:

Applicant gratefully acknowledges the indication that claims 1, 4, 12 and 14 have been allowed.

Claim Rejections Under 35 U.S.C §102:

Claim 36 is rejected under 35 U.S.C. §102(e) as being anticipated by **Fukase** (U.S.P. 5,728,596).

This rejection is respectfully traversed.

Claim 36 has a feature that the first insulation film is in contact with the side walls of the conductor patterns. That is, the first insulation film is formed on the side walls of the conductor patterns with no sidewall insulation film interposed there between. This structural feature means that the sidewall insulation film is formed after the formation of the contact hole and the etching stopper film is subjected to only one etching process to form the sidewall insulation film. According to this

feature, the etching damage (including a decrease in thickness) subjected to the etching stopper film can be lowered, whereby the etching stopper film can be thinned and the patterning of the conducting film and the etching stopper film to form the conductor patterns with the etching stopper film formed thereon can be simplified.

In **Fukase**, the first sidewall layer 10 and the embedded insulating layer 11 are formed on the side wall of the gate electrode 4 in the first etching-back step (FIGs. 2B-2C). Then, the interlayer insulating layer 13 and the contact hole 15 are formed (FIG. 2E), Next, the second sidewall layer 17 is formed on the side walls of the gate electrode 4 and the contact hole 15 in the second etching-back step (FIGs. 2F-2G). Thus, the etching stopper layer 7 is subjected to two etching steps to form the sidewall layers 10, 17. The thickness of the etching stopper layer is decreased by each of the steps. Thus, the thickness of the etching stopper layer must be thickened in consideration of the decrease in thickness in the etching-back steps. When the thick etching stopper layer is formed on the conducting layer to be the gate electrode, the thick laminated layer must be patterned to form the gate electrode. Thus, the processing accuracy of the gate electrode is deteriorated. It therefore is difficult to fill the space between the gate electrodes by the insulation film. In **Fukase**, the interlayer insulating film 13 is formed on the side walls of the gate electrode 4 with the sidewall layer 10 interposed there between. Thus, the claimed invention is clearly different from **Fukase**. The above-described effects achieved by the present inventions cannot be obtained by the structure of **Fukase**. **Fukase** neither teaches nor suggests the claimed structure. Thus, the claimed structure would have been unobvious to one of ordinary skill in the art.

As described above, **Fukase** is clearly different from the present invention and does not provide any motivation for the present invention.

Claim Rejections Under 35 U.S.C. §102(e):

Claims 2, 3, 7 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by **Hosotani et al**. (U.S.P. 5,799,583).

This rejection is respectfully traversed.

Similarly to claim 36, claim 2, and its dependent claims have a feature that the first insulation film is in contact with the side walls of the conductor patterns. This structural feature means that the sidewall insulation film is formed after the formation of the contact hole. According to this feature, it is unnecessary that the sidewall insulation film is used as the etching stopper to form the contact hole, so that the sidewall insulation film can be formed of the material other than silicon nitride that is generally used as the etching stopper material and has a higher dielectric constant than silicon oxide. Thus, according to the claimed invention, the transistor can have a higher hot carrier immunity and the parasitic capacitance can be lowered (see page 40, line 19 to page 41, line 1 of the specification of the present application).

In **Hosotani**, the sidewalls 21 are formed before the formation of the BPSG film 22 and the contact hole, so that the sidewalls 21 are formed on both sides of the gate electrodes 19 and the

BPSG firm 22 is formed on the side walls of the gate electrodes 19 with the sidewall 21 interposed there between (see FIGs. 6-11), Thus, the claimed invention is clearly different from **Hosotani**. The above-described effects achieved by the present inventions cannot be obtained by the structure of **Hosotani**. **Hosotani** neither teaches nor suggests that the sidewalls 21 are formed after the formation of the contact hole. Thus, the claimed structure would have been unobvious to one of ordinary skill in the art.

As described above, **Hosotani** is clearly different from the present invention and does not provide any motivation for the present invention.

Claim Rejections Under 35 U.S.C. §103:

Claims 5 and 6 are rejected under 35 U.S.C. §103(a) as being unpatentable over **Hosotani et al.**, in further view of **Fukase**.

This rejection is respectfully traversed.

As described above, **Fukase** and **Hosotani** are clearly different from the present invention and do not provide any motivation for the present invention. Thus, the claimed invention would have been unobvious to one of ordinary skill in the art, even though **Fukase** and **Hosotani** are combined.

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made
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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/050,113

IN THE CLAIMS:

Claims 2 and 36 as follows have been AMENDED to read as follows:

2. (Five Times Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including a plurality of conductor patterns adjacent to each other;

an etching stopper film covering an upper surface of the conductor patterns;

a contact hole located in a part of a region between the adjacent conductor patterns and having an end thereof defined by the conductor patterns;

a first insulation film which is filling spaces between said plurality of conductor patterns where the contact hole is not formed and not extending over the etching stopper film, the first insulation film being in contact with side walls of the conductor patterns; and

a sidewall insulation film formed on an inner wall of the contact hole so that the side walls of the conductor pattern and the etching stopper film are covered.

36. (Thrice Amended) A semiconductor device comprising:

a base substrate;

a first conducting film formed over the base substrate and including two conductor patterns adjacent to each other;

an etching stopper film covering each upper surface of the two conductor patterns;

a first insulation film formed over the etching stopper film and the base substrate, the first insulation film being in contact with the side walls of the two conductor patterns;

a contact hole, located between the two conductor patterns, reaching the base substrate through the first insulation film, wherein an end of the contact hole is positioned on the etching stopper film; and

a sidewall insulation film formed on an inner wall of the first insulation film, each side wall of the two conductor patterns, and each side wall of the etching stopper film in the contact hole, in which

the end of the contact hole is defined by four sides including a first pair of sides which are opposed to each other and a second pair of sides which are opposed to each other,

the first pair of sides is defined by the conductor patterns,

the second pair of sides is defined by the first insulation film.